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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,339	03/13/2001	Yo Ng Zhou	SNSY-A2000-016	3843

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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/808,339	Applicant(s) ZHOU ET AL.	
	Examiner Thai Phan	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a)☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4)☐ Interview Summary (PTO-413) Paper No(s). _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION

This Office Action is in response to patent application S/N: 09/808,339. Claims 1-23 are now pending.

Drawings

Informal drawings submitted on 03/13/2001 are acceptable for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent no. 6,339,836 B1 issued to Eisenhofer et al.

As per claim 1, Eisenhofer discloses a method and system for simulating circuit design with feature limitations very similar to the claimed invention. According to Eisenhofer, the method includes steps

Accessing an input netlist describing the integrated circuit design (Summary of the Invention) wherein the netlist organized in a hierarchical fashion,

In response to an event, determining a group of leaf cells of the netlist that are effected by the event (col. 5, line 50 to col. 6, line 3, cols. 10-12, for example),

Dividing the group of leaf cells into stages based on hierarchical boundaries as defined in the netlist (Fig. 7, col. 12, lines 29-63, for example),

Converting or transforming each of the stages into separate circuit model or representation for simulation (col. 12, lines 4-28),

Using the circuit models or representations to simulate node voltages of the partitioned stages and recording the result of computation in memory,

And repeating the steps above for other partitions. Eisenhofer does not expressly disclose cut node as claimed.

Practitioner in the art at the time of the invention was made would have found Eisenhofer disclosure of circuit node partition as above would imply the claimed limitation of cut node because the partition process cuts the hierarchy design into a set of cut nodes for a portion of the design, for example.

As per claim 2, Eisenhofer discloses circuit models for simulation. Such models would include Thevenin equivalent model as claimed.

As per claim 3, Eisenhofer discloses state event as claimed (col. 5, line 52 to col. 6, line 3, for example).

As per claims 4-6, Eisenhofer discloses stage changes for a group of stages (col. 5, line 52 to col. 6, line 28, for example) would imply sensitivity stage vector as claimed.

As per claim 7, Eisenhofer discloses a folded representation for circuit partition. Such folded representation would imply cell reuse in order to save memory as disclosed in col. 9, lines 8-20.

As per claim 8, Eisenhofer discloses the circuit netlist for cell connectivities.

As per claim 9, Eisenhofer discloses a method and system for simulating circuit design with feature limitations very similar to the claimed invention. According to Eisenhofer, the system includes method steps:

Accessing an input netlist describing the integrated circuit design (Summary of the Invention) wherein the netlist organized in a hierarchical fashion,

In response to an event, determining a group of leaf cells of the netlist that are effected by the event (col. 5, line 50 to col. 6, line 3, cols. 10-12, for example),

Dividing the group of leaf cells into stages based on hierarchical boundaries as defined in the netlist (Fig. 7, col. 12, lines 29-63, for example),

Converting or transforming each of the stages into separate circuit model or representation for simulation (col. 12, lines 4-28),

Using the circuit models or representations to simulate node voltages of the partitioned stages of the circuit under design and recording the result of computation in memory,

And repeating the steps above for other partitions. Eisenhofer does not expressly disclose cut node using the Thevenin model as claimed.

Practitioner in the art at the time of the invention was made would have found Eisenhofer disclosure of circuit node partition using circuit simulation model as above would imply the claimed limitation of cut node using the node voltage model as Thevenin because the simulators in the circuit simulation models the circuit by node voltage models such as Thevenin model and the simulator processes the partition of

circuit model by cutting the circuit hierarchy design into set of cut nodes for node voltage simulation.

As per claim 10, Eisenhofer discloses state event as claimed (col. 5, line 52 to col. 6, line 3, for example).

As per claims 11-14, Eisenhofer discloses stage changes for a group of stages (col. 5, line 52 to col. 6, line 28, for example) would imply sensitivity stage vector as claimed. Eisenhofer also discloses a folded representation for circuit partition. Such folded representation would imply cell reuse in order to save memory as disclosed in col. 9, lines 8-20. The result of circuit simulation is stored in the memory (col. 6, lines 29-63).

As per claim 15, Eisenhofer discloses a method and computerized system for simulating circuit design with feature limitations very similar to the claimed invention. According to Eisenhofer, the method includes steps

Accessing an input netlist describing the integrated circuit design (Summary of the Invention) wherein the netlist organized in a hierarchical fashion,

In response to an event, determining a group of leaf cells of the netlist that are effected by the event (col. 5, line 50 to col. 6, line 3, cols. 10-12, for example),

Dividing the group of leaf cells into stages based on hierarchical boundaries as defined in the netlist (Fig. 7, col. 12, lines 29-63, for example),

Converting or transforming each of the stages into separate circuit model or representation for simulation (col. 12, lines 4-28),

Using the circuit models or representations to simulate node voltages of the partitioned stages and recording the result of computation in memory,

And repeating the steps above for other partitions. Eisenhofer does not expressly disclose cut node as claimed.

Practitioner in the art at the time of the invention was made would have found Eisenhofer disclosure of circuit node partition as above would imply the claimed limitation of cut node because the partition process cuts the hierarchy design into a set of cut nodes.

As per claim 16, Eisenhofer discloses a plurality of circuit models for simulation. Such models would include Thevenin equivalent model known in the art as claimed.

As per claim 17, Eisenhofer discloses state event as claimed (col. 5, line 52 to col. 6, line 3, for example).

As per claims 18-20, Eisenhofer discloses stage changes for a group of stages (col. 5, line 52 to col. 6, line 28, for example) would imply sensitivity stage vector as claimed. The simulator also simulates circuit design characteristics such as node circuit voltages, node states, etc.

As per claims 21-22, Eisenhofer discloses a folded representation for circuit partition. Such folded representation would imply cell reuse in order to save memory as disclosed in col. 9, lines 8-20.

As per claim 23, Eisenhofer discloses netlist for cell connectivities.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,838,947, issued to Darin, Harish, on Nov. 1998
2. US patent no. 6,108,494, issued to Eisenhofer et al., on Aug. 2000
3. US patent no. 6,446,239 B1, issued to Markosian et al., on Sept. 2002
4. US patent no. 6,449,761 B1, issued to Greidinger et al., on Sept. 2002

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 703-305-3812

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Thai Phan
Jan. 25, 2004

ThaiPhan
Thai Phan
Patent Examiner
AU: 2128